CLAIMS

What is Claimed is:

1. A conditional access module, for controlling access to a media program via a receiver communicably coupleable to the conditional access module, comprising:

a first processor;

a second processor; and

an interface module, communicatively coupled to the first processor and the second processor, the interface module for processing all communications with the conditional access module and externally manifesting a single virtual processor to the receiver.

2. The apparatus of claim 1, wherein the first processor performs a subset of functions to control access to the media program and the second processor performs a second subset of functions to control access to the media program.

3. The apparatus of claim 1, wherein:

the first processor is communicatively coupled a first processor memory;

the second processor is communicatively coupled to a second processor memory; and

wherein the first processor memory is isolated from the second processor and the second processor memory is isolated from the first processor.

4. The apparatus of claim 1, wherein the interface module comprises:

a first module for receiving conditional access module messages; and

a second module for interpreting the received messages and for generating first processor messages for the first processor and second processor messages for the second processor from the received messages.

5. The apparatus of claim 4, wherein the interface module comprises:

a third module for receiving a first set of response messages generated by the first processor and a second set of response messages generated by the second processor; and

a fourth module for generating conditional access module response messages using at least a portion of the first set of response messages and at least a portion of the second set of response messages.

6. The apparatus of claim 1, wherein the interface module receives messages from the receiver, interprets the received messages, and generates first processor messages for the first processor and second processor messages for the second processor.

7. The apparatus of claim 6, wherein the first processor and second processor operate independently and the interface module generates first processor messages for the first processor and second processor messages for the second processor by alternately directing received messages to the first processor and the second processor.

8. The apparatus of claim 6, wherein the first processor messages and the second processor messages define a functional allocation between the first processor and the second processor, and wherein the functional allocation is time-varying.

9. The apparatus of claim 8, wherein the functional allocation is time varied according to a clock.

10. The apparatus of claim 8, wherein the received messages include encrypted data and the functional allocation is time varied according to the encrypted data.

11. The apparatus of claim 6, wherein the interface module receives a first set of response messages generated by the first processor and a second set of response messages generated by the second processor and generates conditional access response messages using at least a portion of the first set of response messages and at least a portion of the second set of response messages.

12. The apparatus of claim 1, wherein the interface processor is a processor.

13. The apparatus of claim 1, wherein the interface processor is a hardware state machine.

14. The apparatus of claim 1, wherein the first processor and the second processor are communicatively coupled to a shared charge pump.

15. The apparatus of claim 1, wherein the first processor and the second processor are communicatively coupled to a shared programming control module.

16. The apparatus of claim 1, wherein the first processor and the second processor each include it's own separate components selected from the group comprising:

voltage supply;

clock;

coprocessor;

read only memory; and

random access memory.

17. The apparatus of claim 1, wherein the first processor and the second processor include separate logical address ranges.

18. The apparatus of claim 1, wherein the first processor and the second processor include separate physical address ranges.

19. A method of controlling access to a media program, comprising the steps of:

receiving a message in a conditional access module from a receiver, the message comprising encrypted information to be decrypted by operations independently performed by a both a first processor and a second processor in the conditional access module;

generating first processor commands and second processor commands from the message;

providing the first processor commands to the first processor and the second processor commands to the second processor;

receiving a first processor response from the first processor;

receiving a second processor response from the second processor; and

generating a conditional access message response from at least a portion of the first processor response and the second processor response.

20. The method of claim 19, wherein the encrypted information is a control word packet and the conditional access message response is a control word.

21. The method of claim 19, wherein first processor and the second processor operate independently and wherein the step of generating first processor commands and second processor commands from the message comprises the steps of:

alternately directing received messages to the first processor and the second processor.

22. The method of claim 21, wherein the first processor messages and the second processor messages define a functional allocation between the first processor and the second processor and wherein the functional allocation is time varying.

23. The method of claim 22, wherein the functional allocation is time varied according to a clock received externally from the conditional access module.

24. The method of claim 22, wherein the received messages include encrypted data and the functional allocation is time varied according to the encrypted data.

25. An apparatus for controlling access to a media program, comprising:

means for receiving a message in a conditional access module from a receiver, the message comprising encrypted information to be decrypted by operations independently performed by a both a first processor and a second processor in the conditional access module;

means for generating first processor commands and second processor commands from the message;

means for providing the first processor commands to the first processor and the second processor commands to the second processor;

means for receiving a first processor response from the first processor;

means for receiving a second processor response from the second processor; and

means for generating a conditional access message response from at least a portion of the first processor response and the second processor response.

26. The apparatus of claim 25, wherein the encrypted information is a control word packet and the conditional access message response is a control word.